New Claims

35. (New) An integrated circuit comprising:

a transistor level comprising one or more semiconductor devices disposed over a substrate and an overlying transistor isolation layer having one or more contact vias extending therethrough;

a ferroelectric structure, positioned over the transistor isolation layer, that includes one or more ferroelectric capacitors, the ferroelectric structure including,

a ferroelectric device level and overlying ferroelectric isolation layer having one or more vias extending therethrough,

a first metal layer, and

an inter-level dielectric level disposed over the first metal level; and

a second metal disposed over the inter-level dielectric level.

36. (New) An integrated circuit, as defined in claim 35, wherein:

the ferroelectric device level, being disposed over the transistor isolation layer, including the one or more ferroelectric capacitors; and

the first metal level disposed over the ferroelectric device level.

37. (New) An integrated circuit, as defined in claim 36, wherein the contact vias are filled with tungsten contact plugs.

38. (New) An integrated circuit, as defined in claim 37, wherein the ferroelectric capacitors are formed over respective tungsten contact plugs.

39. (New) An integrated circuit, as defined in claim 36, wherein the vias of the ferroelectric isolation layer being laterally sized larger than the corresponding contact vias aligned therewith.

40. (New) An integrated circuit, as defined in claim 39, wherein the contact vias are filled with tungsten contact plugs.

41. (New) An integrated circuit, as defined in claim 40, wherein the ferroelectric capacitors are formed over respective tungsten contact plugs.

42. (New) An integrated circuit, as defined in claim 35, wherein:

the first metal level and ferroelectric device level are integrated and positioned over the transistor isolation layer, the integrated first metal level and ferroelectric device level including first metal contacts, and

the inter-level dielectric level is disposed over the integrated first metal level and ferroelectric device level.

43. (New) An integrated circuit, as defined in claim 42, wherein the contact vias are filled with tungsten contact plugs.

44. (New) An integrated circuit, as defined in claim 43, wherein the ferroelectric capacitors are formed over respective tungsten contact plugs.

45. (New) An integrated circuit, as defined in claim 42, wherein the integrated first metal and ferroelectric device level has a thickness corresponding substantially to the ferroelectric capacitor heights.

46. (New) An integrated circuit, as defined in claim 42, wherein the integrated first metal and ferroelectric device level is substantially non-planar with a reduced thickness in non-capacitor regions.

47. (New) An integrated circuit, as defined in claim 35, wherein:

the first metal level disposed over the transistor isolation layer; and

the ferroelectric device level, including the one or more ferroelectric capacitors, being positioned over the first metal level.

48. (New) An integrated circuit, as defined in claim 47, wherein the contact vias are filled with tungsten contact plugs.

49. (New) An integrated circuit, as defined in claim 48, wherein the ferroelectric capacitors are formed over respective tungsten contact plugs.

50. (New) An integrated circuit, as defined in claim 35, wherein:

the first metal level disposed over the transistor isolation layer; and

the ferroelectric device level, including the one or more ferroelectric capacitors, disposed over the inter-level dielectric level.

51. (New) An integrated circuit, as defined in claim 50, wherein the contact vias are filled with tungsten contact plugs.

52. (New) An integrated circuit, as defined in claim 51, wherein the ferroelectric capacitors are formed over respective tungsten contact plugs.

53. (New) A method of forming an integrated circuit, comprising:

forming a transistor level comprising one or more semiconductor devices disposed over a substrate and an overlying transistor isolation layer having one or more contact vias extending therethrough;

forming a ferroelectric structure, positioned over the transistor isolation layer, that includes one or more ferroelectric capacitors, the ferroelectric structure including,

a ferroelectric device level and overlying ferroelectric isolation layer having one or more vias extending therethrough,

a first metal layer, and

an inter-level dielectric level; and

forming a second metal level over the ferroelectric device level.

54. (New) A method of forming an integrated circuit, as defined in claim 53, comprising:

forming the ferroelectric device level over the transistor isolation layer, the ferroelectric device level including the one or more ferroelectric capacitors; and

forming the first metal level over the ferroelectric device level.

55. (New) A method of forming an integrated circuit, as defined in claim 54, wherein the contact vias are filled with tungsten contact plugs.

56. (New) A method of forming an integrated circuit, as defined in claim 55, wherein the ferroelectric capacitors are formed over respective tungsten contact plugs.

57. (New) A method of forming an integrated circuit, as defined in claim 54, wherein the vias of the ferroelectric isolation layer being laterally sized larger than the corresponding contact vias aligned therewith.

58. (New) A method of forming an integrated circuit, as defined in claim 57, wherein the contact vias are filled with tungsten contact plugs.

59. (New) A method of forming an integrated circuit, as defined in claim 58, wherein the ferroelectric capacitors are formed over respective tungsten contact plugs.

60. (New) A method of forming an integrated circuit, as defined in claim 53, comprising:

forming an integrated first metal level and ferroelectric device level over the transistor isolation layer, the integrated first metal level and ferroelectric device level including first metal contacts, and

forming the inter-level dielectric level over the integrated first metal level and ferroelectric device level.

61. (New) A method of forming an integrated circuit, as defined in claim 60, wherein the contact vias are filled with tungsten contact plugs.

62. (New) A method of forming an integrated circuit, as defined in claim 61, wherein the ferroelectric capacitors are formed over respective tungsten contact plugs.

63. (New) A method of forming an integrated circuit, as defined in claim 60, wherein the integrated first metal and ferroelectric device level has a thickness corresponding substantially to the ferroelectric capacitor heights.

64. (New) A method of forming an integrated circuit, as defined in claim 60, wherein the integrated first metal and ferroelectric device level is substantially non-planar with a reduced thickness in non-capacitor regions.

65. (New) A method of forming an integrated circuit, as defined in claim 53, comprising:

forming the first metal level over the transistor isolation layer; and

forming the ferroelectric device level, including the one or more ferroelectric capacitors, over the first metal level.

66. (New) A method of forming an integrated circuit, as defined in claim 65, wherein the contact vias are filled with tungsten contact plugs.

67. (New) A method of forming an integrated circuit, as defined in claim 66, wherein the ferroelectric capacitors are formed over respective tungsten contact plugs.

68. (New) A method of forming an integrated circuit, as defined in claim 53, comprising:

forming the first metal level over the transistor isolation layer; and

forming the ferroelectric device level, including the one or more ferroelectric capacitors, over the inter-level dielectric level.

69. (New) A method of forming an integrated circuit, as defined in claim 68, wherein the contact vias are filled with tungsten contact plugs.

70. (New) A method of forming an integrated circuit, as defined in claim 69, wherein the ferroelectric capacitors are formed over respective tungsten contact plugs.